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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,172	12/30/2003	Jae-Won Han	OPP 031047 US	3390
36872	7590	05/31/2006	EXAMINER	
THE LAW OFFICES OF ANDREW D. FORTNEY, PH.D., P.C. 401 W FALLBROOK AVE STE 204 FRESNO, CA 93711-5835			LEE, KYOUNG	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

AD

Office Action Summary	Application No.	Applicant(s)	
	10/751,172	HAN, JAE-WON	
	Examiner	Art Unit	
	Kyoung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 15 March 2006.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-7,9-14 and 17-23 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-7,9-14 and 17-23 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 30 December 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Drawings

The drawings are objected to because figures 3A-3D needs "Prior Art" label. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: In line 4 of the paragraph [0002] of Description of the Related Art, Applicants recite "STI (swallow

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trench isolation)". The examiner suggests replacing "STI (shallow trench isolation)". In line 1 of the paragraph [0004] of Description of the Related Art, Applicants recite "to the prior arts". The examiner suggests replacing "to the prior art". In line 3 of the paragraph [0007] of Description of the Related Art, Applicants recite "the semiconductor substrate 10". The examiner suggests replacing "the semiconductor substrate 100". In line 1 of the paragraph [0009] of Description of the Related Art, Applicants recite "the prior arts". The examiner suggests replacing "the prior art". In line 1 of the paragraph [0021] of Brief Description of the Drawings, Applicants recite "according to the prior arts". The examiner suggests replacing "according to the prior art". In line 4 of the paragraph [0025] of Brief Description of the Preferred Embodiment, Applicants recite "ploy 16". The examiner suggests replacing "poly 16". In line 6 of the paragraph [0029] of Brief Description of the Preferred Embodiment, Applicants recite "Fig. 2d". The examiner suggests replacing "Fig. 2D". In line 4 of the paragraph [0034] of Brief Description of the Preferred Embodiment, Applicants recite "Silicide 30 with". The examiner suggests replacing "Silicide 30' with". In line 2 of the paragraph [0035] of Brief Description of the Preferred Embodiment, Applicants recite "silicide 30 is". The examiner suggests replacing "silicide 30' is". The examiner suggests replacing "Silicide 30' with". In line 4 of the paragraph [0036] of Brief Description of the Preferred Embodiment, Applicants recite "silicide 30 can". The examiner suggests replacing "silicide 30' can".

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is

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requested in correcting any errors of which applicant may become aware in the specification.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Applicant does not describe the word "monosilicide". Applicant should include the word monosilicide to describe CoSi.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 2-4, 11-14, 18, and 21-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 2, 14, 18, and 23 are rejected because they contain new matter "comprises CoSi" or "comprises CoSi₂". In the specification only "with a composition ratio of CoSi" is disclosed. Claims 3-4, 11-13, 21-22 depend from claims 2, 14, 18, or 23 so they are rejected for the same reason. This new matter was added in the first amendments filed on 9/29/05. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamanaka (U.S. patent No. 6,337,272) in view of Raaijmakers (U.S. patent No. 4,908,331).

Referring to Figs. 1A-2B and corresponding text, Hamanaka discloses (Re claim 1) a method of manufacturing silicide, comprising the steps of: (a) cleaning a semiconductor substrate with a transistor formed thereon, the transistor including a source electrode, a drain electrode and a gate electrode (b) placing the cleaned semiconductor substrate into a sputter chamber in a deposition equipment, and (c) forming silicide at the same time of depositing a metal film under a state where the semiconductor substrate is heated at a temperature from 200 to 500°C (see col. 2, lines 25-42), approximately 450C (see par. bridging cols. 9-10); (d) removing residual metal film not used for the formation of silicide; and (e) annealing the semiconductor substrate (see col. 8, lines 7-60 and col. 9, line 40-col. 10, line 13). But it fails to disclose expressly the heating the semiconductor substrate to a temperature range and then initially forming a monosilicide at the same time as depositing a metal film.

Raaijmakers discloses the method of forming monosilicide by depositing metal on the surface while heating the semiconductor body to a temperature at which metal

silicide is formed during the deposition (see figures 1-2 and column 2 line 34 through column 4 line 43). It would have been obvious to one of ordinary skill in the art at the time the invention was made to initially forming a monosilicide at the same time as depositing a metal film in the method of Hamanaka in order to reduce the process time of forming monosilicide.

[Re claims 2] Hamanaka also discloses wherein, in the step (c), the silicide comprises CoSi (see column 9, line 15 through column 10, line 13).

[Re claims 12] Hamanaka also discloses wherein, the step (e) includes heating the semiconductor substrate during a predetermined duration at a temperature of more than 500°C in a RTP equipment (see column 5, lines 40-62).

[Re claims 14] Hamanaka also discloses wherein, after the step (e) the silicide comprises CoSi₂ (see col. 9, line 15 through column 10, line 13).

Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over "Hamanaka" in view of "Raaijmakers" and O'Brien et al. (U.S. Patent No. 6,458,711).

The combined teachings of Hamanaka and Raaijmakers disclose substantially the limitations of claims 3-4, as shown above. Hamanaka also discloses [Re claim 4] wherein the step (a) includes a second cleaning step comprising cleaning the semiconductor substrate with HF or DHF solution (see column 8, lines 7-15). But Hamanaka and Raaijmakers fail to disclose expressly [Re claim 3] wherein the step (a) includes a first cleaning step comprising cleaning the semiconductor substrate with SC1 solution. However, the missing limitation is well known in the art because O'Brien

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discloses this feature (See col. 3, lines 40-55). A person of ordinary skill is motivated to modify Hamanaka with O'Brien to clean undesirable metallic material. Therefore, at the time of the invention, it would have been obvious to combine Hamanaka with Raaijmakers and O'Brien to obtain the invention as specified in claims 3-4.

Claims 5-7, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamanaka in view of Raaijmakers and Sumi (U.S. Patent No. 6,022,805).

The combined teachings of Hamanaka and Raaijmakers disclose substantially the limitations of claims 5-7, and 10, as shown above. But Hamanaka and Raaijmakers fail to disclose expressly the details about the dry etching. However, the missing limitations are well known in the art because Sumi discloses the use of Ar for sputtering etch with flow rates of 20sccm or 2sccm and power of about 500W, the conditions can vary depending on the amount of oxide to be etched, the exposed features, and acceptable duration (See column 10, lines 3-11 and column 12, lines 40-49). A person of ordinary skill is motivated to modify Hamanaka with Sumi to obtain a desired surface oxide etch with damaging the critical dimensions of exposed features. Therefore, at the time of the invention, it would have been obvious to combine Hamanaka with Raaijmakers and Sumi to obtain the invention as specified in claims 5-7, and 10.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over, as "Hamanaka" in view of "Raaijmakers" and Wake (U.S. Patent No. 6,725,119).

The combined teachings of Hamanaka and Raaijmakers disclose substantially the limitations of claims 11, as shown above. But Hamanaka and Raaijmakers fail to disclose expressly wherein, the step (d) includes a first removal step of removing the metal film for 5-15 minutes in SPM solution at a temperature of 50-150°C and a second removal step comprising removing the metal film for 3-10 minutes in SCI solution at a temperature of 40-70°C. However, the missing limitations are well known in the art because Wake discloses the etching in SPM and SCI (APM) (See column 17, line 57 through column 18, line 38). Wake does not disclose the duration and temperatures. However, it would have been obvious for an ordinary skill to use conventional etchants to etch at a temperature and duration to achieve the cleanliness required for a specific process. A person of ordinary skill is motivated to modify Hamanaka with Wake to use conventional etchants with known characteristics. Therefore, at the time of the invention was made, it would have been obvious to combine Hamanaka with Raaijmakers and Wake to obtain the invention as specified in claim 11.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over, as "Hamanaka" in view of "Raaijmakers" and Wang et al. (U.S. Patent No. 5,780,362).

The combined teachings of Hamanaka and Raaijmakers disclose substantially the limitations of claims 1and 13, as shown above. But Hamanaka and Raaijmakers fail to disclose wherein the step (e) includes heating the semiconductor substrate for 20-60 minutes at a temperature of 500-900°C in an electric furnace. Wang discloses the method including heating the semiconductor substrate for 20-60 minutes at a

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temperature of 500-900°C in an electric furnace (see column 3, lines 63-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to heating the semiconductor substrate for 20-60 minutes at a temperature of 500-900°C in an electric furnace in the method of Hamanaka in order to convert CoSi₂ from monosilicide.

Claims 9, 17-18, 21, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over, as "Hamanaka" in view of "Raaijmakers" and Fortin et al. (U.S. Patent Appl. No. 2003/0148606 A1).

[Re claims 9 and 17] The combined teachings of Hamanaka and Raaijmakers disclose substantially the limitations of claims 9 and 17, as shown above. But Hamanaka and Raaijmakers fail to disclose wherein the step (b) comprises sputtering cobalt at a DC power of 2-10 KW. Fortin discloses the method wherein comprising sputtering cobalt at a DC power of 2 KW. It would have been obvious to one of ordinary skill in the art at the time the invention was made to sputtering cobalt at a DC power of 2 KW in order to penetrate the barrier formed by thermal energy. Therefore, at the time of the invention was made, it would have been obvious to combine Hamanaka with Raaijmakers and Wake to obtain the invention as specified in claims 9 and 17.

[Re claims 18] Hamanaka also discloses wherein the silicide comprises CoSi (see column 9, line 15 through column 10, line 13).

[Re claims 21] Hamanaka also discloses wherein, the step (d) includes heating the semiconductor substrate during a predetermined duration at a temperature of more than 500°C in a RTP equipment (see column 5, lines 40-62).

[Re claims 23] Hamanaka also discloses wherein, after the step (d) the silicide comprises CoSi₂ (see col. 9, line 15 through column 10, line 13).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hamanaka in view of Raaijmakers, Fortin and Sumi (U.S. Patent No. 6,022,805).

The combined teachings of Hamanaka, Raaijmakers, and Fortin disclose substantially the limitations of claims 17 and 19, as shown above. But Hamanaka, Raaijmakers, and Fortin fail to disclose expressly the details about the dry etching. However, the missing limitations are well known in the art because Sumi discloses the use of Ar for sputtering etch with flow rates of 20sccm or 2sccm and power of about 500W, the conditions can vary depending on the amount of oxide to be etched, the exposed features, and acceptable duration (See column 10, lines 3-11 and column 12, lines 40-49). A person of ordinary skill is motivated to modify Hamanaka with Sumi to obtain a desired surface oxide etch with damaging the critical dimensions of exposed features. Therefore, at the time of the invention, it would have been obvious to combine Hamanaka with Raaijmakers, Fortin, and Sumi to obtain the invention as specified in claim 19.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over, as "Hamanaka" in view of "Raaijmakers", "Fortin", and Wake (U.S. Patent No. 6,725,119).

The combined teachings of Hamanaka, Raaijmakers, and Fortin disclose substantially the limitations of claims 17 and 20, as shown above. But Hamanaka, Raaijmakers, and Fortin fail to disclose expressly wherein, the step (d) includes a first removal step of removing the metal film for 5-15 minutes in SPM solution at a temperature of 50-150°C and a second removal step comprising removing the metal film for 3-10 minutes in SCI solution at a temperature of 40-70°C. However, the missing limitations are well known in the art because Wake discloses the etching in SPM and SCI (APM) (See column 17, line 57 through column 18, line 38). Wake does not disclose the duration and temperatures. However, it would have been obvious for an ordinary skill to use conventional etchants to etch at a temperature and duration to achieve the cleanliness required for a specific process. A person of ordinary skill is motivated to modify Hamanaka with Wake to use conventional etchants with known characteristics. Therefore, at the time of the invention was made, it would have been obvious to combine Hamanaka with Raaijmakers and Wake to obtain the invention as specified in claim 20.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over, as "Hamanaka" in view of "Raaijmakers", "Fortin" and Wang et al. (U.S. Patent No. 5,780,362).

The combined teachings of Hamanaka, Raaijmakers, and Fortin disclose substantially the limitations of claims 18 and 22, as shown above. But Hamanaka Raaijmakers, and Fortin fail to disclose wherein the step (d) includes heating the semiconductor substrate for 20-60 minutes at a temperature of 500-900°C in an electric furnace. Wang discloses the method including heating the semiconductor substrate for 20-60 minutes at a temperature of 500-900°C in an electric furnace (see column 3, lines 63-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to heating the semiconductor substrate for 20-60 minutes at a temperature of 500-900°C in an electric furnace in the method of Hamanaka in order to convert CoSi₂ from monosilicide.

Response to Arguments

In view of arguments and the amendment to the claims, the rejections of claims 1-7, 9-14, and 17-23 under 35 U.S.C. 103, as stated in the immediately preceding Office Action, have been withdrawn.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kyoung Lee whose telephone number is (571) 272-1982. The examiner can normally be reached on M-F 8:30AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KL 5/30/05



MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER